

IN THE CLAIMS

✓ Please cancel claim 1 without prejudice or disclaimer and  
 ✓ add new claims 37-41 as set forth below.

*A3 SUB B17*  
 --37. A semiconductor memory apparatus comprising:  
 a semiconductor memory device comprising a source region and a drain region, a semiconductor current path connected between the source and the drain regions, a plurality of small memory nodes covered by a potential barrier over the periphery of the memory nodes, a control electrode controlling a voltage of the current path and the memory nodes;

a plurality of the semiconductor memory devices storing an information by a difference of an electron charge in each memory node;

a plurality of control gates connected to each other between the plural semiconductor memory devices; and

wherein a voltage applied between the source and the drain in the semiconductor memory device is different according to the difference in information to be written in a writing operation in the plural semiconductor memory device.

--38. The semiconductor memory device according to claim 37, wherein a large voltage among the voltage applied between

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--41. The semiconductor memory device according to claim 37, wherein the current path is located on the insulator film.--

Claim 1 has been canceled without prejudice or disclaimer. New claims 37-41 have been added. Accordingly, claims 37-41 are currently pending in the application.

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